High Temperature, Wafer-Level Capacitance Measurements in Lake Shore Cryogenic Probe Stations

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Variable-temperature capacitance measurements can be used to approximate the charge distribution in solid state depletion regions, but rely on precise temperature-dependent calibrations. The capacitance calibration drift in a Lake Shore CRX-4K probe station, high temperature stage, parametric probes, and a Keysight B1500A operating at 600 K is shown to be less than 0.1% over nearly 40 min for a 30 pF capacitor. Measurement drift is attributed to temperature drift in the probe after calibration. The resulting calibration is used to confirm an ultra-wide bandgap diode's doping density at several temperatures.

Introduction

Capacitance-voltage (C-V) and capacitance-frequency (C-F) measurements are common and powerful tools used to characterize charge and charge dynamics in electronic materials and solid state electronic devices. Capacitance, a measure of charge storage, is defined by:

$$C = \partial Q / \partial V \quad (1)$$

C-V measurements can be used to resolve charge Q and can be used to approximate the ionized dopant density as a function of depth with a spatial resolution of a few Debye lengths [1]. Variable temperature C-V measurements allow one to approximate the charge profile as a function of temperature, and find dopant/defect ionization energies and the onset of high intrinsic carrier concentrations [2]. Variable-temperature C-F measurements offer insight into loss mechanisms and their relative time constants [2]. Broad temperature characterization has applications for material quality and reliability testing [1], cryo-cooled detectors and electronics [3], studying the high temperature performance of wide and ultra-wide bandgap (WBG and UWBG) materials and devices [4], and in many other fields.

Using a Keysight B1500A and a Lake Shore C-V probing kit, two-terminal C-V measurements are typically carried out from 4 K to 350 K in a Lake Shore CRX-4K probe station. The C-V probing Kit, which features cryogenically-compatible parametric probes, allows the shields of the two probes to be shorted together in proximity to the DUT—completing the shield path and creating a more precise capacitance measurement. Elevated device temperatures, to 675 K, are achieved in the CRX-4K station with the addition of a high temperature stage; however, the simultaneous use of parametric probes and the high temperature stage prevent the radiation shield lid from fitting over the experimental space. In this work, the radiation shield lid was removed (Fig. 1A) to accommodate the height of the parametric probes. Without the radiation shield lid, the base temperature of the high temperature stage is raised from below 20 K to approximately 23 K.

Calibration

C-V measurements are commonly made at 1 MHz [1] and require calibration for high sensitivity. Cables, probes, and the probe station itself create a network of parasitic circuit elements, translating the measurement reference plane away from the device, as depicted in Fig. 1C. Calibration routines, built in to the Keysight B1500A, use measurements of short and open loads to move the measurement plane back from the extrinsic reference plane to the intrinsic one. This calibration is vital for accurately resolving capacitances on the order of tens of picofarads or smaller. Calibration is typically performed by using a short standard or by shorting the probes together on a conducting pad (for example, a metal pad on the UWBG diode shown in Fig. 1B) and by lifting the probes above the circuit to create an open circuit. The probes are then landed on the sample to make a measurement. The parasitic circuit elements associated with the probe, however, have temperature-dependent values. Landing the probe allows for rapid heat transfer between the sample and probes, heating the probes, altering the parasitic elements, and causing a calibration shift. Poor calibration stability can damage measurement accuracy and repeatability.

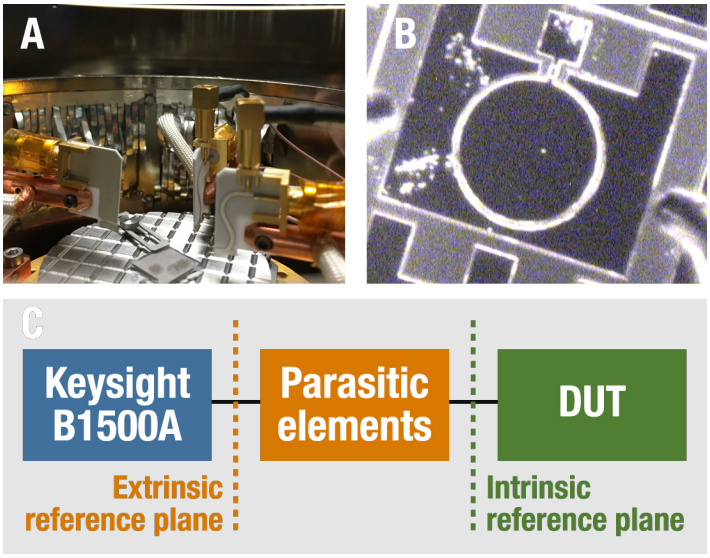

Fig. 1: (A) Lake Shore CRX-4K probe station with parametric probes and no radiation shield; (B) UWBG $Al_{0.7}Ga_{0.3}N$ diode with probe tips nearby; and (C) block diagram showing the difference between the extrinsic and intrinsic planes

Calibration stability was analyzed at 600 K in a CRX-4K probe station. A Keysight B1500A was calibrated at time t = 0. 1 MHz C-F measurements of a 30 pF UWBG circular diode were taken regularly for approximately 40 min. The measured capacitance after time t = 0 was compared to the capacitance measured at later times; significant deviations from a ratio of 1.00 indicates that the calibration significantly drifted as the probe's temperature

changed. The resulting study was performed for a ~1 K probe arm temperature change (Fig. 2A) and a ~15 K probe arm temperature change (Fig. 2B).

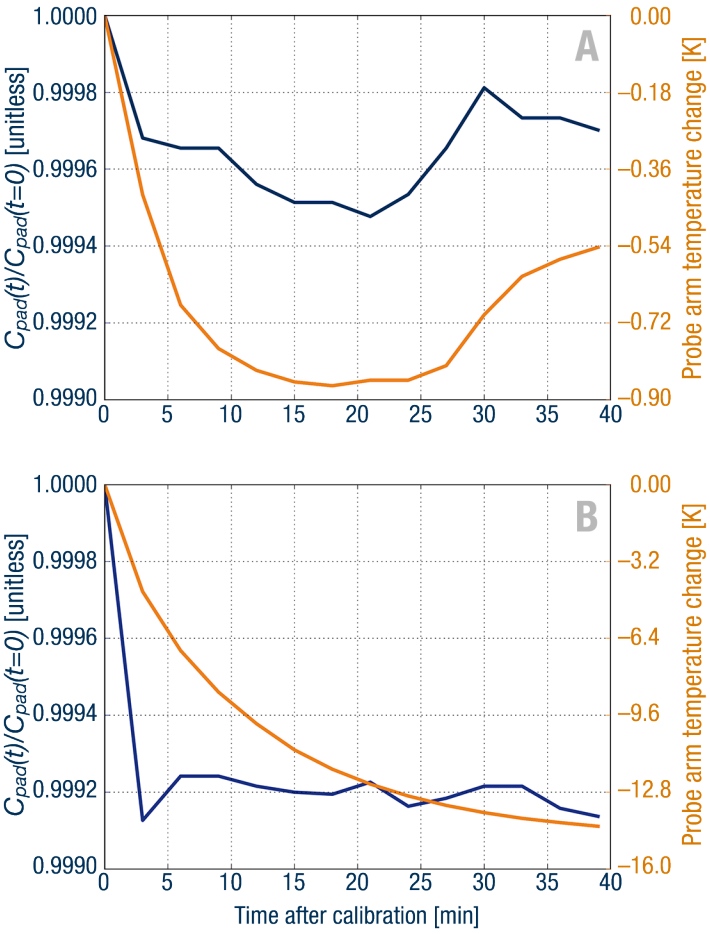

Fig. 2: Calibration drift with rising temperature for (A) ~1 K drift and (B) ~15 K drift; the calibration drift is on the order of 0.05% (A) and 0.1% (B), indicating minimal drift in a 40 min measurement

The calibration drift in both cases occurs during the largest change in probe arm temperature and is on the order of 0.1% or less, even after nearly 40 min of measurement. In both Fig. 2A and 2B, the capacitance converges after the probe arm temperature begins to stabilize and any additional drift correlates strongly with a change in temperature. This drift is approximately 15 fF, which is small for the diode studied here. A 15 fF shift, however, would render the capacitance of modern silicon FETs nearly immeasurable [5]. For extremely sensitive high temperature C-V and C-F measurements, we recommend leaving the probe in contact with the device surface to allow the probe to reach thermal equilibrium. Perform open and short calibrations and immediately make the necessary measurement to avoid small drifts.

Approximating dopant concentrations

One key advantage of UWBG solid state electronics is their low intrinsic carrier concentrations [2], which allows the devices to remain in the extrinsic carrier regime at high temperatures. C-V measurements use a DC voltage bias to modulate the width of the depletion region. Subsequent C-V measurements measure the incremental addition of charge at the edge of the depletion region. By stepping through a variety of DC biases and measuring the capacitance, the magnitude of the charge density can be computed as a function of depth into the depletion region. The charge density may be found by [1]:

$$N_{eff} = \frac{2}{q\epsilon\left|\frac{\partial}{\partial V}\left(\frac{1}{C^2}\right)\right|} \quad (2)$$

In equation 2, q is the electron charge and ϵ is the semiconductor permittivity. The numerical derivative in (2) reduces the measurement accuracy by one order [6] and can lead to noisy N_{eff} estimates. Careful measurement and good calibration are therefore imperative for accurately resolving the charge profile, particularly for small capacitances. The DC bias may be converted to depth t through [1] (where A is the device or material area):

$$t = \frac{\epsilon A}{C(V)} \quad (3)$$

C-V charge-depth profiling was used to estimate the doping density of the UWBG diode shown in Fig. 1B. C-V curves were taken following a separate calibration at each temperature and are shown in Fig. 3A. The inset shows the Q-factor of the measured capacitance and shunt conductance (also commonly measured with capacitance), which should be greater than five for reliable measurements [1]. Fig. 3B shows the variable-temperature approximate ionized acceptor density for the n-type UWBG layer with an expected doping density of 10^{18} cm^{-3}.

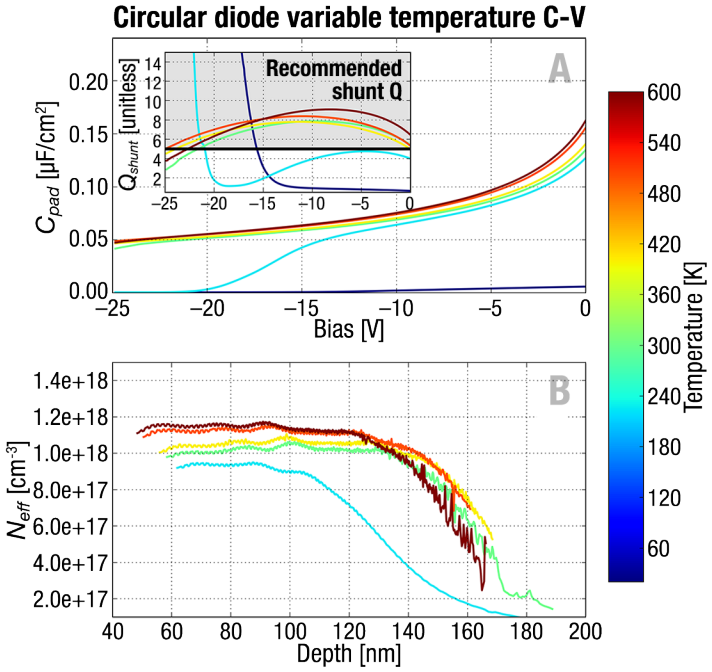

Fig. 3: (A) Variable temperature C-V measurements with (inset) shunt Q and a recommended figure of merit and; (B) Charge-depth profile extracted from panel A

Fig. 3B reveals that the doping density is most nearly 10^{18} cm^{-3} at temperatures of 300 K and above. The measurement made at 225 K reveals a slightly reduced carrier concentration, indicating that some of the impurity states have begun to freeze out. The measurement taken at 23 K (navy colored trace in Fig. 3A) lies outside the scale of Fig. 3B because the impurities are no longer completely ionized, pushing the diode out of the extrinsic carrier regime.

Summary

We explore the use of Lake Shore CRX-4K probe stations, parametric probes, and a high temperature stage option for making C-V and C-F measurements. Careful capacitance calibrations are shown to drift by less than 0.1% over about 40 min at 600 K, even with large swings in the measurement probe tip temperature. The resulting calibrations were used to confirm the doping density in an UWBG diode over a broad variety of temperatures.

Acknowledgment

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